25/03/2019

EE446 LABORATORY

EXPERIMENT 3

PRELIMINARY REPORT

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Tuesday Afternoon

**1.2.1. Datapath Design**

**1.** Instructions need to be fetched with the address of PC from instruction memory. Fetched instructions are fed to control unit, register file and extend module.

PC is incremented by 4.

For LDR, STR and Data processing instructions, the developments on the Datapath is shown in the following figures.

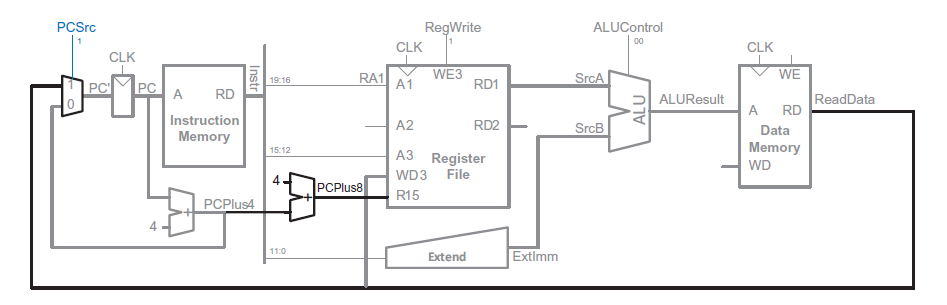


Figure 1 Datapath for LDR instruction

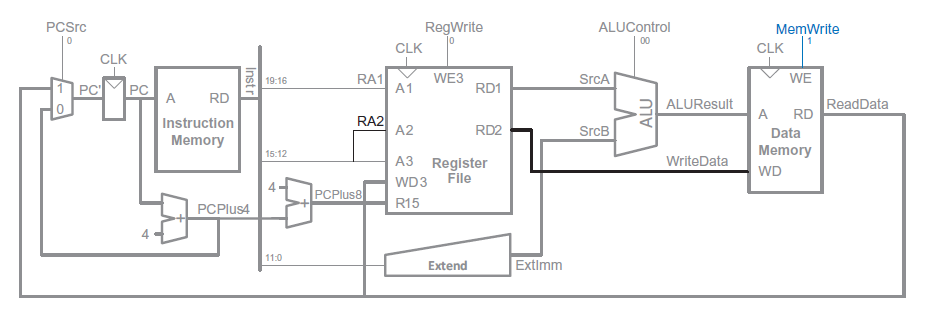


Figure 2 Datapath for STR instruction

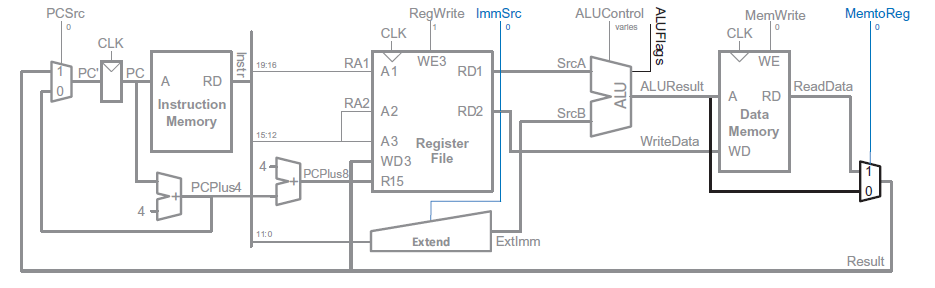


Figure 3 Datapath for Data Processing instructions with immediate addressing mode

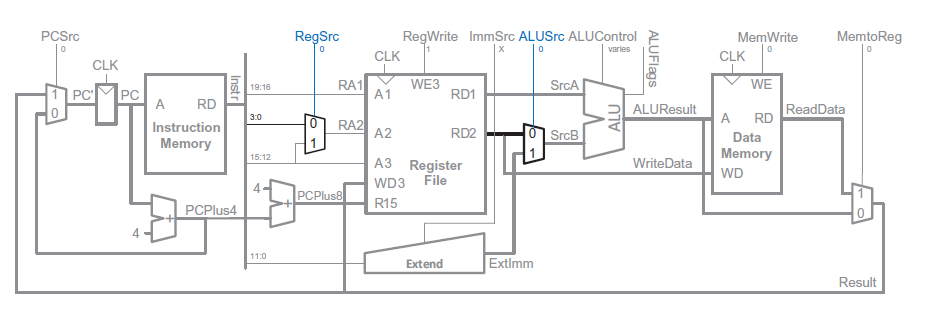


Figure 4 Datapath for Data Processing instructions in register Addressing mode

For LSR and LSL instructions, A shifter module will be added to the 0th input of the SrcB multiplexer and an additional 2x1 multiplexer will be added in front of the input A of the data memory.Therefore shifted version of the RD2 will be directed to data memory or the register file.

**2.**

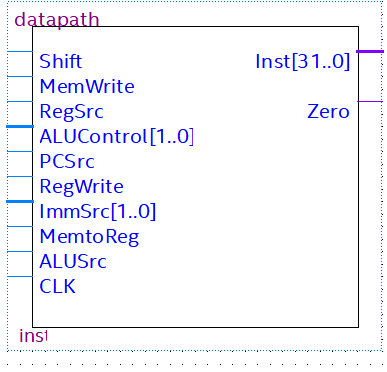


Figure 5 Datapath as a black box

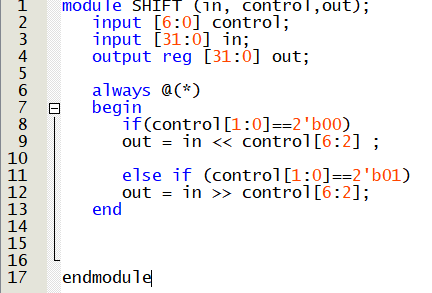


Figure 6 SHIFT module implementation

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**1.2.2. Controller Design**

**1.**

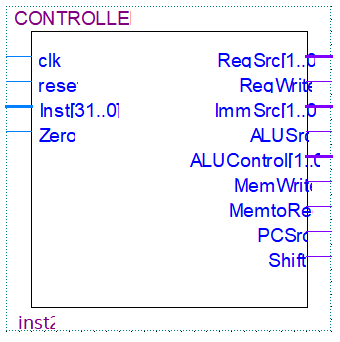


Figure 7 Controller as a black box

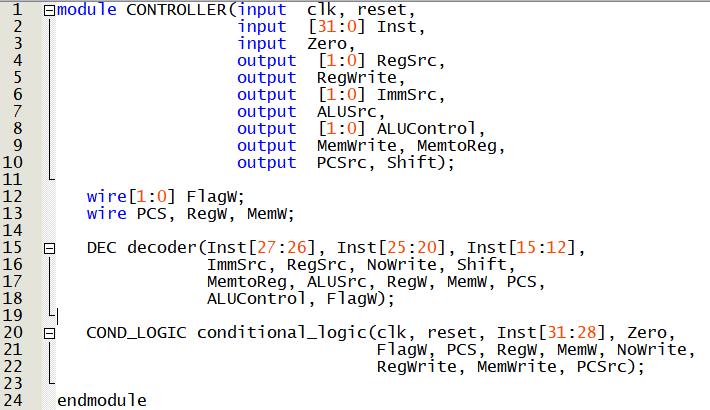
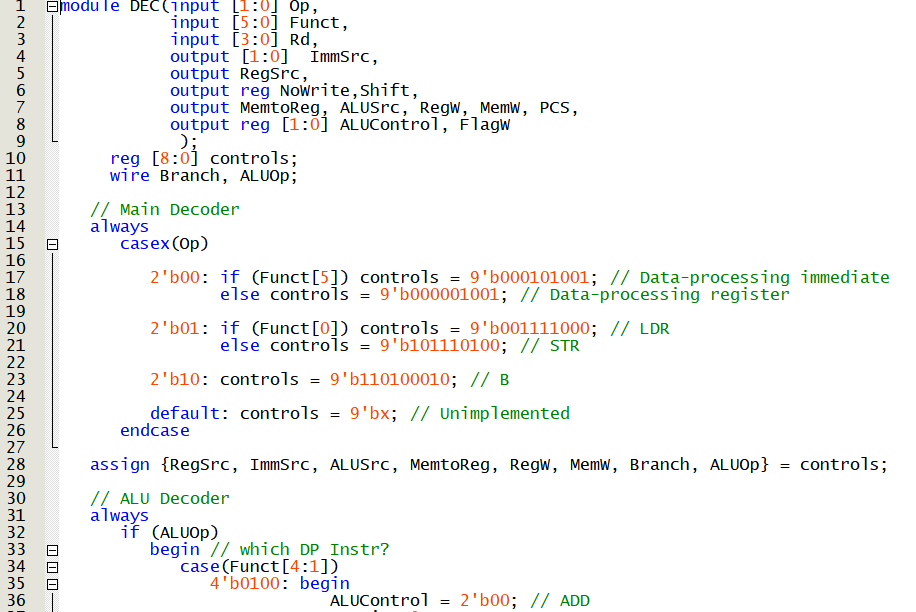
**2.** 

Figure 8 CONTROLLER Module



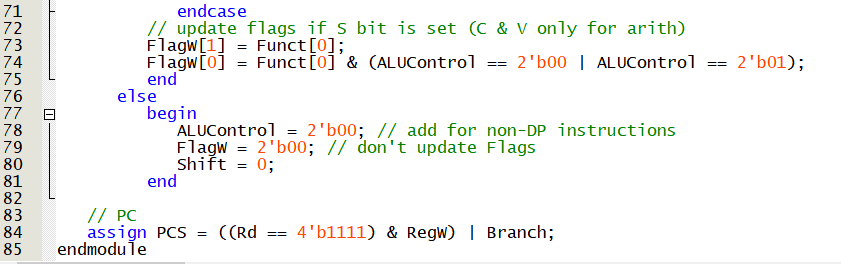
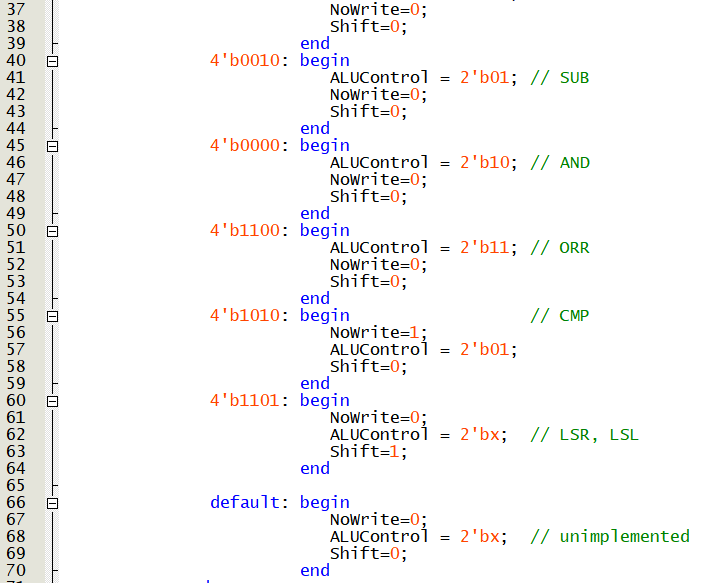


Figure 9 DECODER module

**3.**

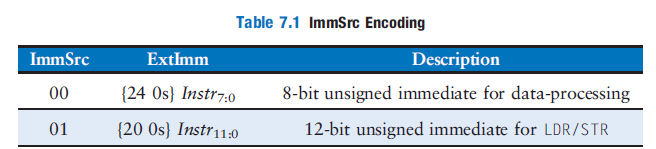


Figure 10 ImmSrc encoding

Table 1 Truth table of the main decoder

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Op | Funct[5] | Funct[0] | Type | MemtoReg | MemW | ALUSrc | ImmSrc | RegW | RegSrc | ALUOp |
| 00 | 0 | X | DP Reg | 0 | 0 | 0 | XX | 1 | 00 | 1 |
| 00 | 1 | X | DP Imm | 0 | 0 | 1 | 00 | 1 | X0 | 1 |
| 01 | X | 0 | STR | X | 1 | 1 | 01 | 0 | 10 | 0 |
| 01 | X | 1 | LDR | 1 | 0 | 1 | 01 | 1 | X0 | 0 |

Table 2 Truth table of the ALU decoder

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| ALUOp | Funct[4:1] | Funct[0] | Type | ALUControl[1:0] | FlagW[1:0] | Shift |
| 0 | X | X | Not DP | 00 | XX | 0 |
| 1 | 0100 | X | ADD | 00 | XX | 0 |
| 1 | 0010 | X | SUB | 01 | XX | 0 |
| 1 | 0000 | X | AND | 10 | XX | 0 |
| 1 | 1100 | X | ORR | 11 | XX | 0 |
| 1 | 1101 | X | LSx | XX | XX | 1 |